WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device comprising:

a first step of patterning a gate electrode above a semiconductor substrate having an element isolation structure previously formed therein;

a second step of forming sidewalls covering only on both side faces of said gate electrode;

a third step of removing the upper portion of said sidewalls to thereby expose a part of both side faces of said gate electrode; and

a fourth step for introducing an impurity into said gate electrode along a direction tilt-angled to the surface of said semiconductor substrate.

2. The method of fabricating a semiconductor device according to claim 1, wherein, in said fourth step, the tilt-angle introduction of the impurity is carried out a plural number of times while varying the direction thereof.

3. The method of fabricating a semiconductor device according to claim 1, wherein said sidewalls and the element isolation structure formed in said semiconductor substrate are formed using different materials so as to allow said sidewalls and said element isolation structure to exhibit different etch

rates in the removal of the upper portion of said sidewalls in said third step.

4. The method of fabricating a semiconductor device according to claim 1, wherein, after said fourth step, additional sidewalls are again formed so as to entirely cover both side faces of said gate electrode.

5. The method of fabricating a semiconductor device according to claim 3, wherein, after said fourth step, additional sidewalls are again formed so as to entirely cover both side faces of said gate electrode.

6. The method of fabricating a semiconductor device according to claim 1, wherein, in said fourth step, the tilt-angle introduction of the impurity is carried out in the presence of a resist mask having an opening formed in a size which ensures protection of areas for forming source-and-drain regions on both sides of said gate electrode from the tilt-angle introduction of the impurity.

7. The method of fabricating a semiconductor device according to claim 3, wherein, in said fourth step, the tilt-angle introduction of the impurity is carried out in the presence of a resist mask having

an opening formed in a size which ensures protection of areas for forming source-and-drain regions on both sides of said gate electrode from the tilt-angle introduction of the impurity.

8. The method of fabricating a semiconductor device according to claim 1, further comprising:

a fifth step of introducing an impurity to a smaller depth into said areas for forming source-and-drain regions on both sides of said gate electrode, said fifth step being provided after said first step and before said second step; and

a sixth step of introducing an impurity to a larger depth into said areas for forming source-and-drain regions, said sixth step being provided after said second step.

9. The method of fabricating a semiconductor device according to claim 4, further comprising:

a fifth step of introducing an impurity to a smaller depth into said areas for forming source-and-drain regions on both sides of said gate electrode, said fifth step being provided after said first step and before said second step; and

a sixth step of introducing an impurity to a larger depth into said areas for forming source-and-drain regions, said sixth step being provided after said second step.

10. The method of fabricating a semiconductor device according to claim 6, further comprising:

a fifth step of introducing an impurity to a smaller depth into said areas for forming source-and-drain regions on both sides of said gate electrode, said fifth step being provided after said first step and before said second step; and

a sixth step of introducing an impurity to a larger depth into said areas for forming source-and-drain regions, said sixth step being provided after said second step.

11. The method of fabricating a semiconductor device according to claim 8, wherein the tilt-angle introduction of the impurity in said fourth step is carried out at an ion acceleration energy lower than that in the introduction of the impurity in said sixth step.

12. The method of fabricating a semiconductor device according to claim 9, wherein the tilt-angle introduction of the impurity in said fourth step is carried out at an ion acceleration energy lower than that in the introduction of the impurity in said sixth step.

13. The method of fabricating a semiconductor device according to claim 10, wherein the tilt-angle introduction of the impurity in said fourth step is carried out at an ion acceleration energy lower than that in the introduction of the impurity in said sixth step.

14. The method of fabricating a semiconductor device according to claim 1, wherein, in said fourth step, said tilt-angle introduction of the impurity is carried out at an angle of 45°.

15. A method of fabricating a semiconductor device comprising:

a first step of patterning a gate electrode above a semiconductor substrate;

a second step of forming a mask having an opening which allows said gate electrode to be exposed therein; and

a third step of introducing an impurity into said gate electrode along a direction tilt-angled to the surface of said semiconductor substrate, wherein

in said second step, said opening of said mask is formed in a size which ensures protection of areas for forming source-and-drain regions on both sides of said gate electrode from the tilt-angle introduction of the impurity.

16. The method of fabricating a semiconductor device according to claim 15, further comprising:

a fourth step of introducing an impurity to a smaller depth into said areas for forming source-and-drain regions on both sides of said gate electrode, said fourth step being provided after the tilt-angle introduction of the impurity in the third step and is carried out in the presence of said mask used in said third step; and

a fifth step of forming sidewalls only on both side faces of said gate electrode and introducing an impurity to a larger depth into said areas for forming source-and-drain regions.

17. The method of fabricating a semiconductor device according to claim 16, wherein the tilt-angle introduction of the impurity in said third step is carried out at an ion acceleration energy lower than that in the introduction of the impurity in said fifth step.

18. The method of fabricating a semiconductor device according to claim 15, wherein, in said third step, the tilt-angle introduction of the impurity is carried out at an angle of 45°.

19. A semiconductor device comprising:

a gate electrode;

source-and-drain regions;

sidewalls covering only the lower portion of both side faces of said gate electrode; and

a silicide film formed on the exposed surface of said gate electrode, wherein

said gate electrode contains an impurity having a conductivity type same as that of the impurity contained in said source-and-drain regions, and said gate electrode has an impurity concentration larger than that of said source-and-drain regions.

20. The semiconductor device according to claim 19, wherein said silicide film is formed as being extended from the top surface to the upper portion of both side faces of said gate electrode.

21. The semiconductor device according to claim 19, wherein said sidewalls are composed only of an oxide film.

22. A computer program product comprising a computer-readable program code means for allowing a computer to execute a procedure for automatically forming an opening in a resist which covers a semiconductor substrate used for masking thereof in a process of introducing an impurity into a gate electrode along a direction tilt-angled to the surface of said semiconductor substrate,

said opening being formed in a size which ensures protection of areas for forming source-and-drain regions on both sides of said gate electrode from the tilt-angle introduction of the impurity.

23. A computer-readable recording medium having recorded therein a program product,

said program product comprising a computer-readable program code means for allowing a computer to execute a procedure for automatically forming an opening in a resist which covers a semiconductor substrate used for masking thereof in a process of introducing an impurity into a gate electrode along a direction tilt-angled to the surface of said semiconductor substrate,

said opening being formed in a size which ensures protection of areas for forming source-and-drain regions on both sides of said gate electrode from the tilt-angle introduction of the impurity.